KEYSIGHT

主题技术报告：电互连技术报告（13:30—18:00）

“腾讯会议”会议号：744-157-893（密码 221216）

时间	会议内容	报告嘉宾	会议主持
13:30-13:50	1.1 后摩尔时代的 Chiplet 解决方案	刘好朋 芯耀辉 技术支持总监	李永耀 中科院计算所
13:50-14:10	1.2 为各种高性能计算场景而生的 Innolink Chiplet IP 技术	高专 芯动科技首席技术官	
14:10-14:30	1.3 数据中心互连场景及其对应的核心技术	王富 百度 DPU 业务单元负责人	
14:30-14:50	1.4 数据中心下一代单通道 224Gbps 高速互连技术的挑战及测试方案	张晓 是德科技资深数字技术方案工程师	
14:50-15:10	1.5 数据中心超低时延网络	庄严 阿里巴巴高级网络架构师	
15:10-15:30	1.6 基于 ADC/DSP 的高速串行接口物理层的关键技术与研究方法	郑旭强 研究员 中科院微电子所	
15:30-15:50	1.7 先进封装及系统应用的电子设计自动化（EDA）技术展望	蒲菠 博士 德图科技创始合伙人/技术副总经理	
15:50-16:10	1.8 Chiplet 技术与设计挑战	苏周祥 芯和半导体中国区技术总监	
16:10-16:30	1.9 从片上到片间互连：体系结构设计在小芯片系统中的机遇和挑战	尹捷明 南京邮电大学教授、博导，江苏省特聘教授，国家高层次青年人才计划入选者	
16:30-16:50	1.10 时不我待——加速高性能芯片核心高速接口 IP 研发	赵喆 牛芯半导体 产品 VP	
16:50-17:10	1.11 fcBGA/SiP 高端封测业务与 Chiplet 规划	金伟强 苏州锐杰微科技集团副总及首席技术专家	
17:10-17:20	主持人总结发言		

数据中心下一代单通道224Gbps高速互连技术的挑战及测试方案

Xiao Zhang | 张 晓, Solutions Engineer | 技术方案工程师

Dec. 16th , 2022

800G/1.6T 以及单通道 224Gbps技术的驱动力

- 为满足下一代系统带宽需求，以太网互联和光模块的目标是800GbE 和 1.6TbE，下一代交换机芯片的目标是102.4T.
- 实现下一代系统的挑战包括功耗、尺寸和成本，单波或单路更高的速率是解决这些挑战的方向，单路200Gbps或以上的速率对于网络和计算带宽的提升至关重要。

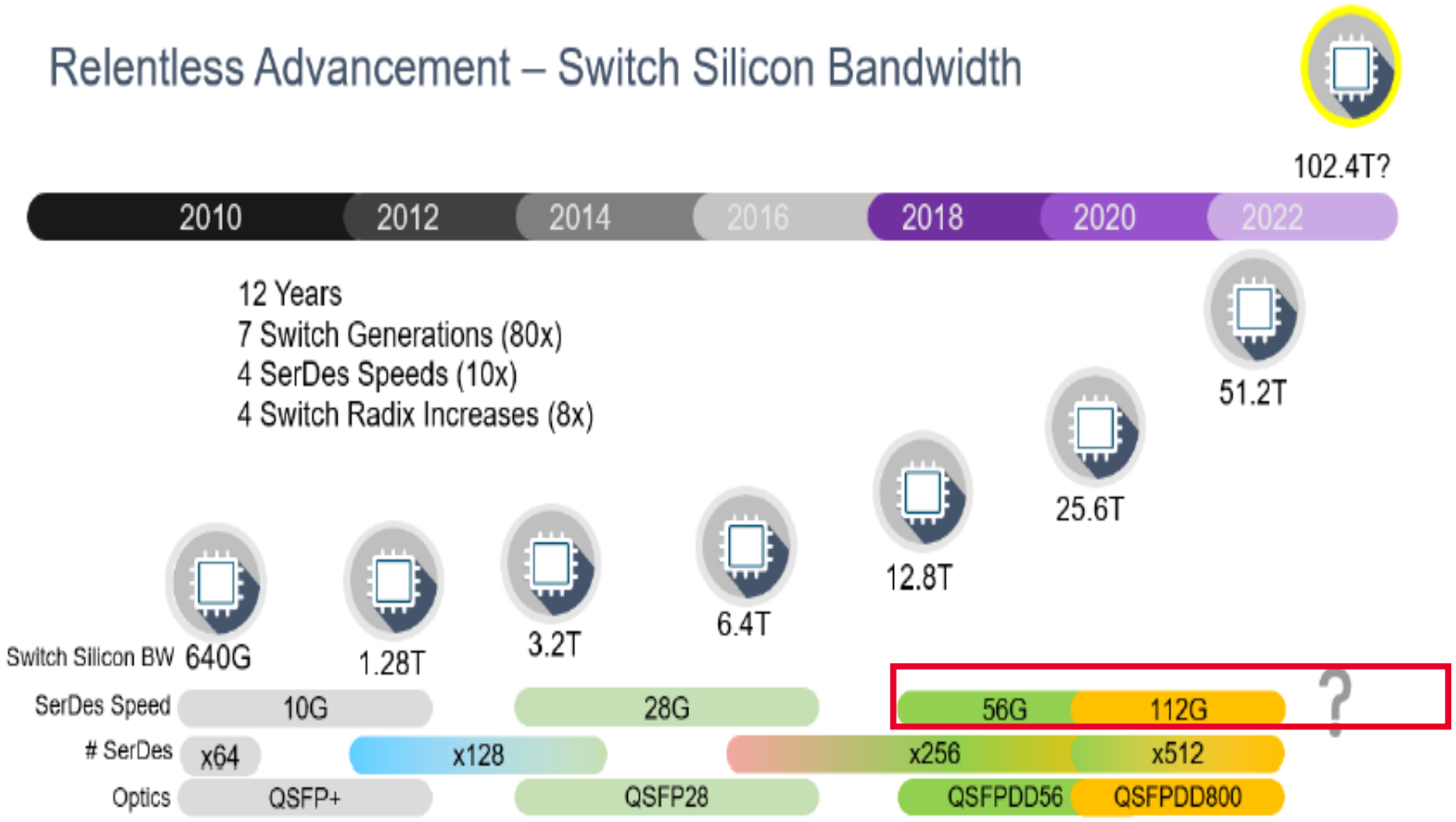
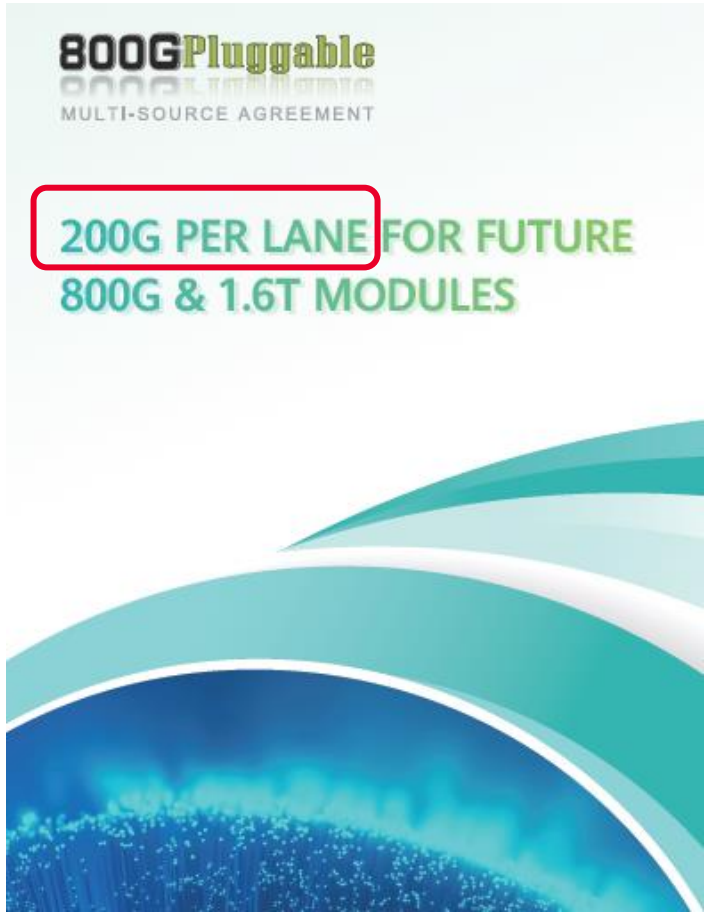


Figure 3 Relentless advancement – switch silicon bandwidth

Source：OIF Next Generation CEI-224G Framework, OIF-FD-CEI-224G-01,February 7, 2022

单通道224G技术

2022年2月，OIF成员启动6个项目，其中4个专用于224G/L。



4个新的CEI项目包括:

1. CEI-224G-Extra Short Reach (XSR) 通用电气封装接口项目;
2. CEI-224G-Very Short Reach (VSR) 通用电气芯片到模块接口项目
3. CEI-224G-中距离(MR)通用电气芯片到芯片接口项目;
4. CEI-224G-Long Reach (LR) 通用电气背板和铜缆接口项目。

OIF

OIF

Next Generation CEI-224G Framework

OIF-FD-CEI-224G-01.0
February 7, 2022

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单通道224G技术的典型应用场景

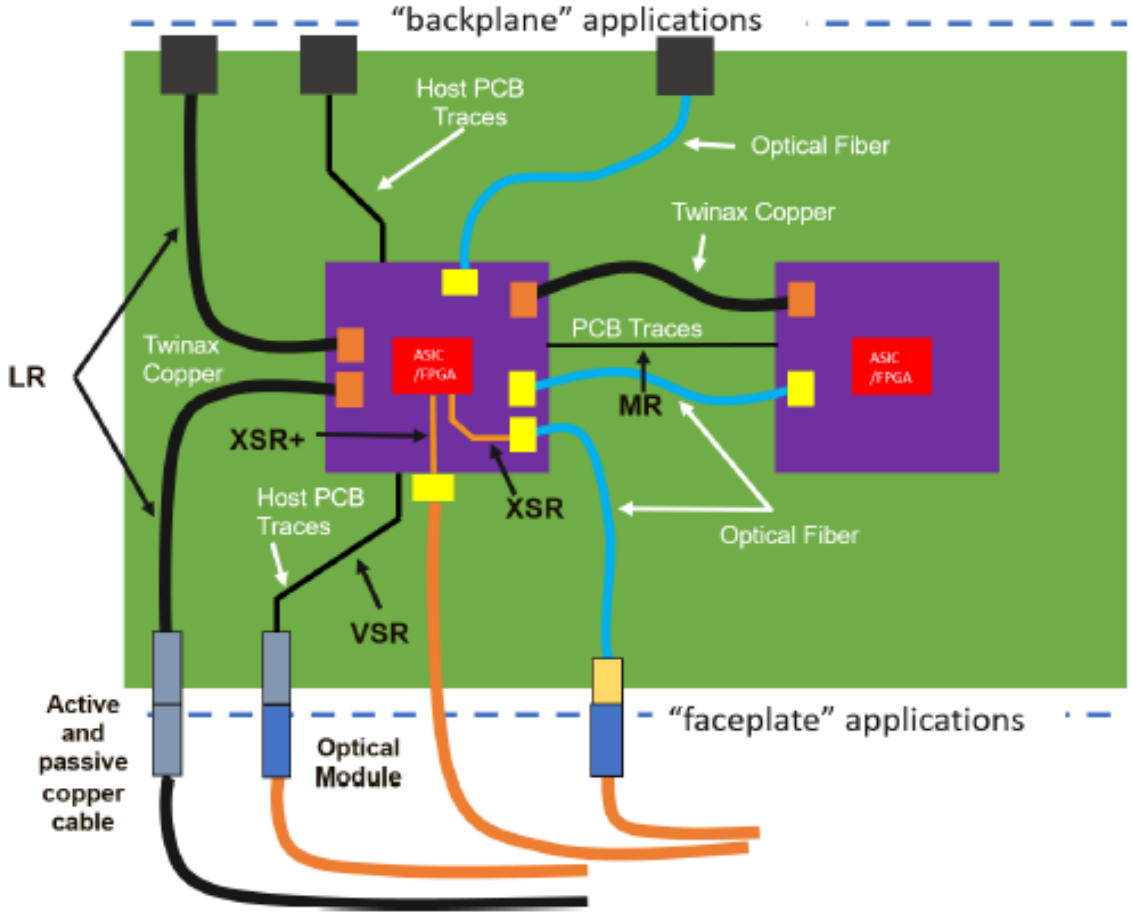
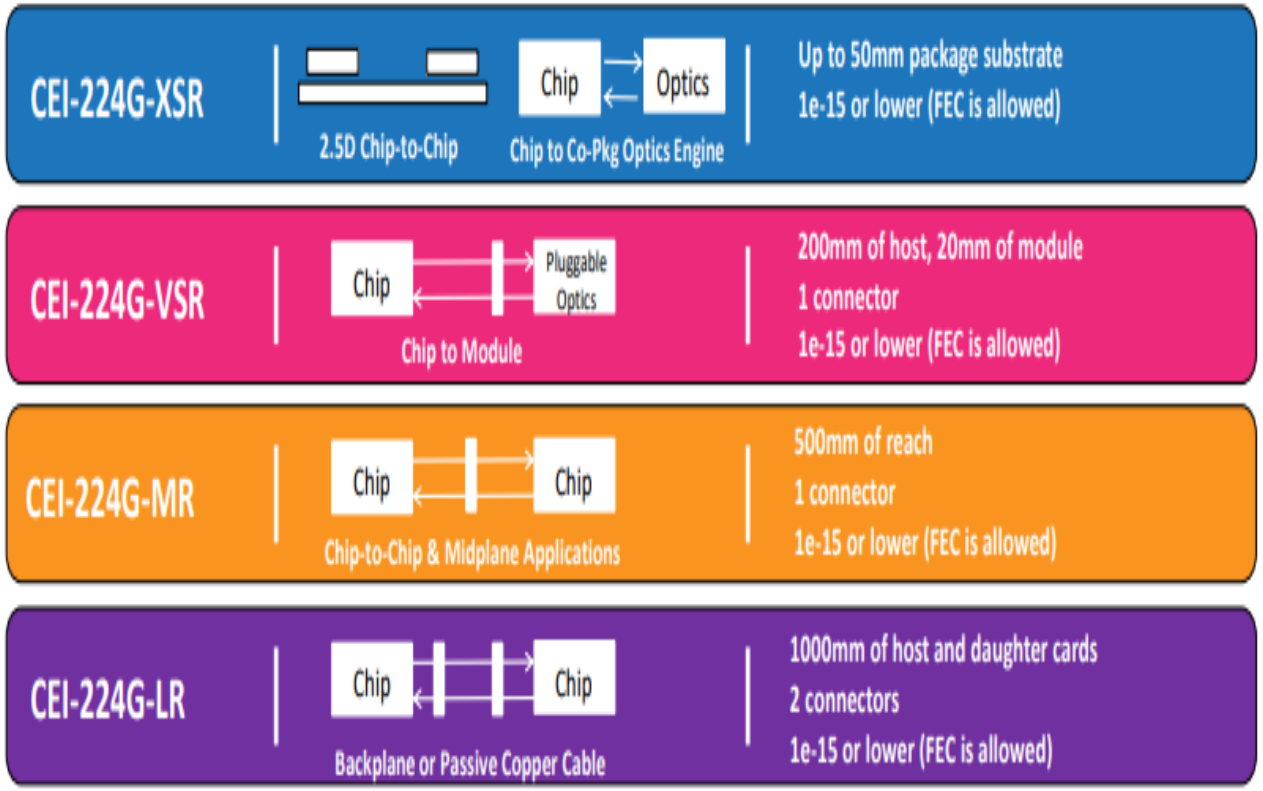


Figure 1 Interconnect Application Spaces



Source：OIF Next Generation CEI-224G Framework, OIF-FD-CEI-224G-01,February 7, 2022

下一代互联技术的挑战

CHALLENGES	POSSIBLE SOLUTION SPACE
POWER DISSIPATION	
I/O DENSITY	
ELECTRICAL LINK REACH	
CHANNEL CHARACTERISTICS	
LINK LATENCY	
DEVICE BANDWIDTH	
TEST and MEASUREMENT	

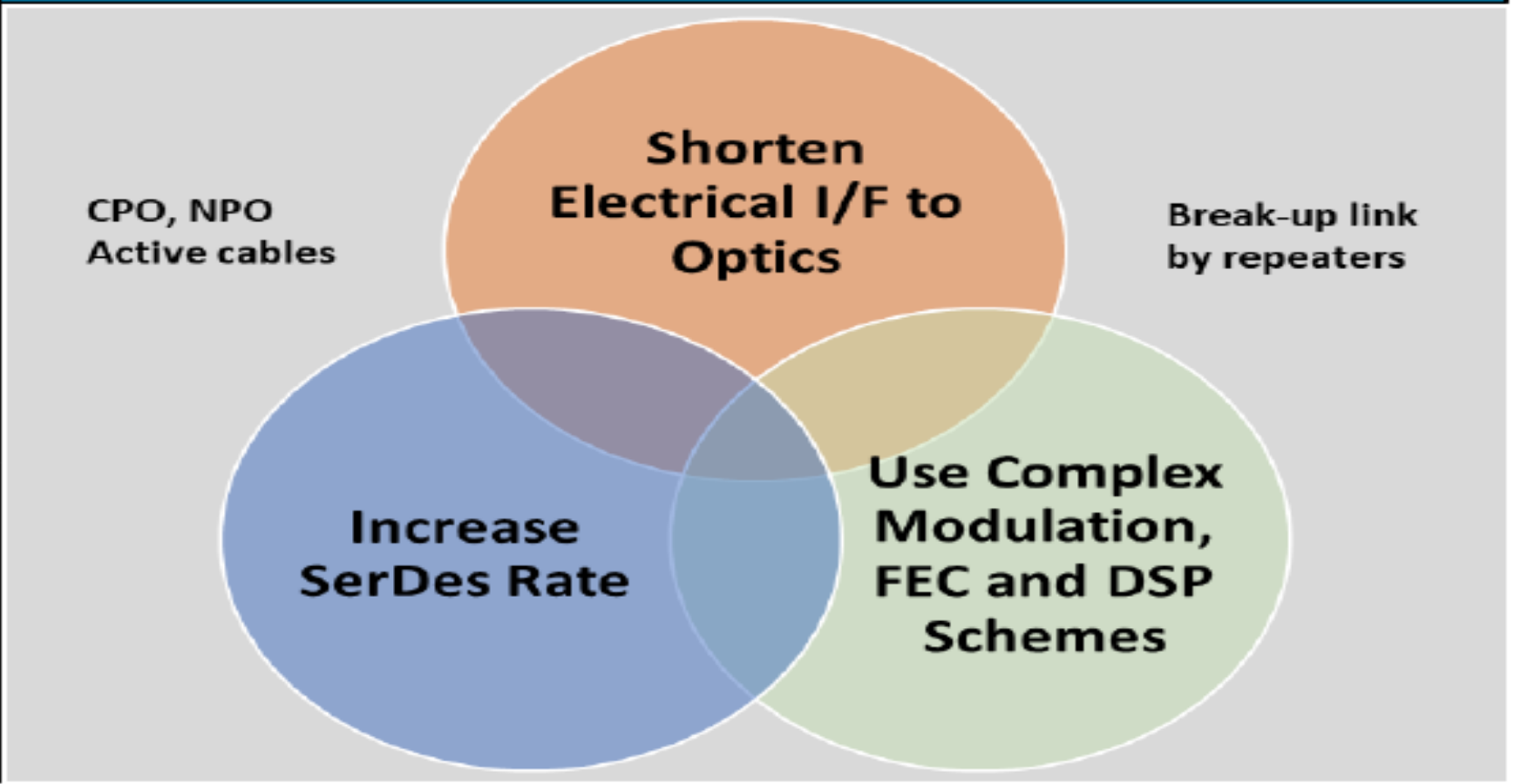


Figure 2 Next generation interconnect challenges

Source：OIF Next Generation CEI-224G Framework, OIF-FD-CEI-224G-01,February 7, 2022

减小系统功耗的方法

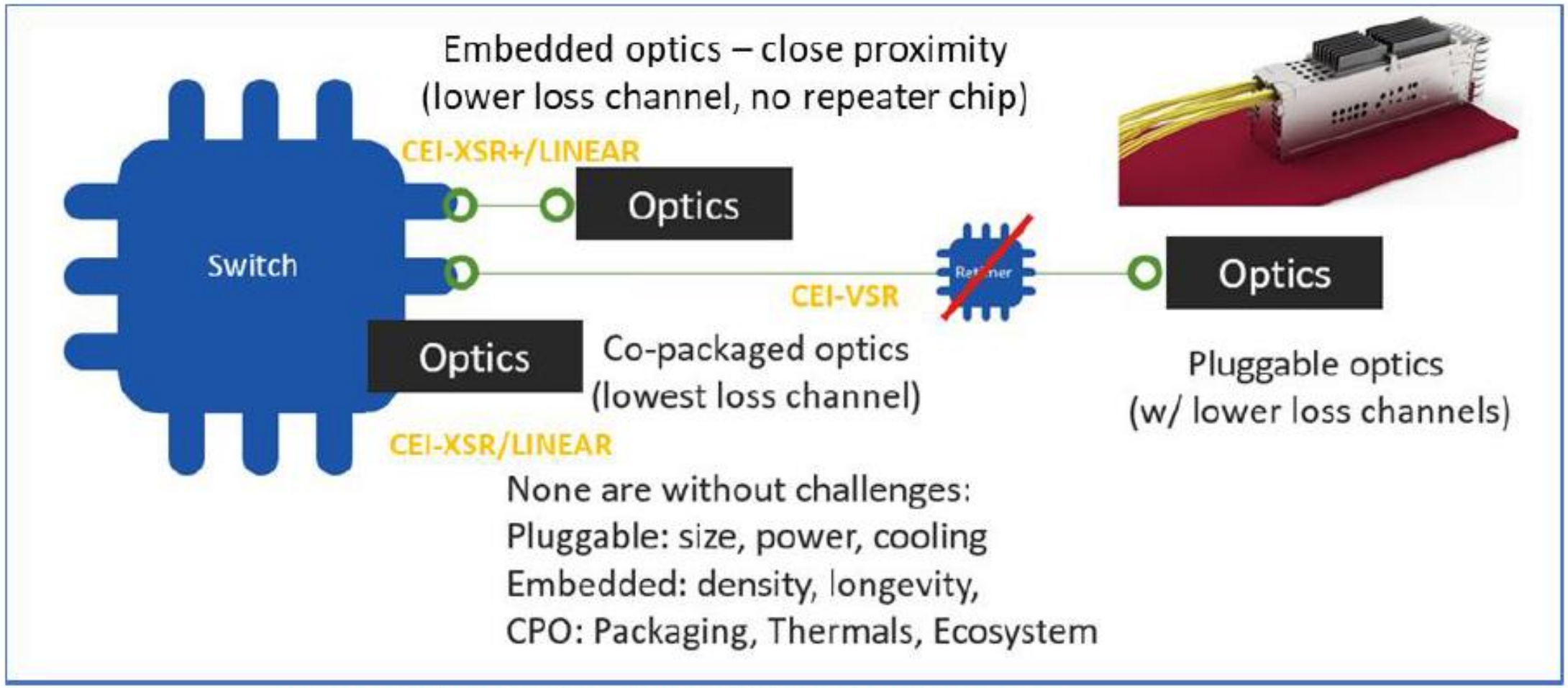
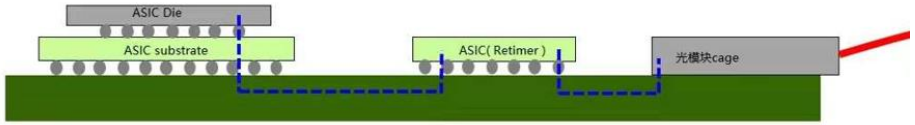


Figure 5 Approaches to minimizing SerDes power

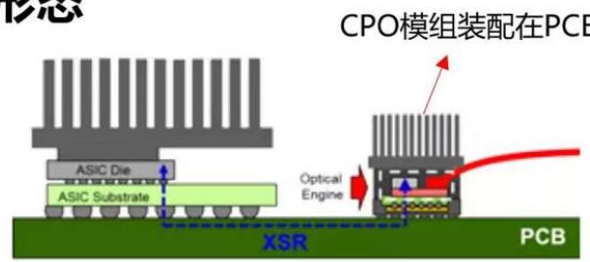
Source：OIF Next Generation CEI-224G Framework, OIF-ED-CEI-224G-01,February 7, 2022

Co-Packaged Optics (CPO) & Near Package Optics (NPO)

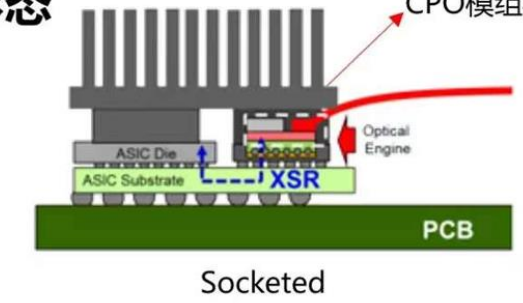
Pluggable形态



NPO形态



CPO形态



Socketed

Pluggable方式：

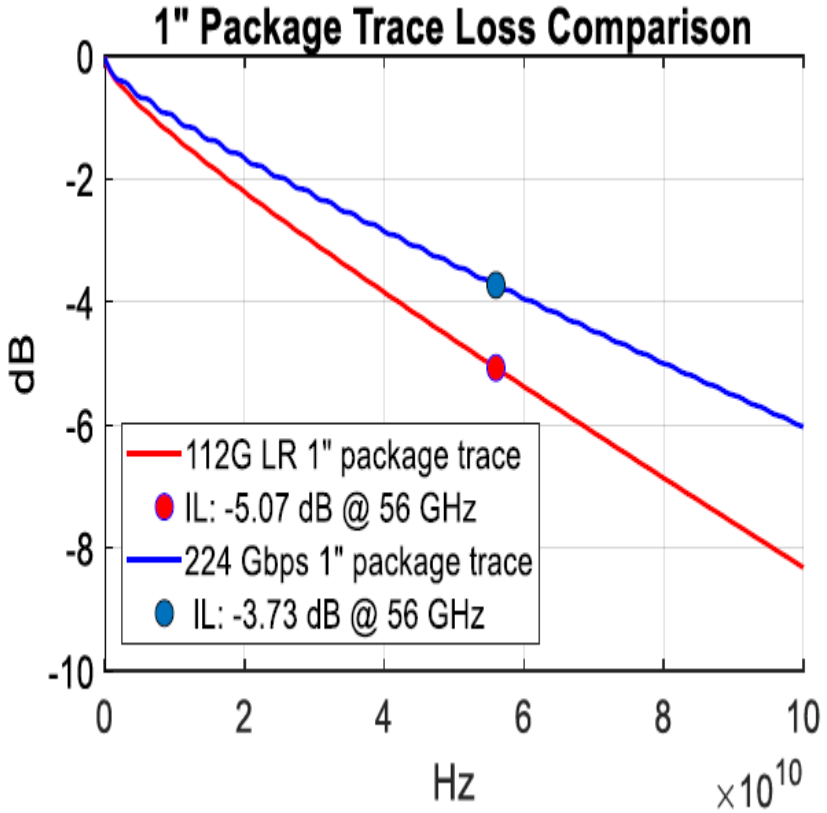
NPO方式：

CPO方式：

CEI–LR Evolution

Table 1 Historical evolution of CEI-LR projects

OIF CEI projects	CEI-25G	CEI-56G	CEI-112G	CEI-224G
Timeline	2011-2014	2014-2018	2018-2021	2021-
Ethernet rate	100G	50/100/200G	100/200/400G	200/400/800/1600G
Switch capacity	3.2T	12.5T	25T/50T	50T/100T
Per-lane data rate	25 Gbps	56 Gbps	112 Gbps	224 Gbps
Modulation	NRZ	PAM4	PAM4	TBD
Insertion loss	25dB at 12.5GHz	30dB at 14GHz	28dB at 28GHz	TBD
Reach objectives	5m copper cable	3m copper cable	2m copper cable	1m coper cable
Pre-FEC BER target	1e-15	1e-4	1e-4	TBD
SerDes architecture	Analog	Analog/DSP	Analog/DSP	TBD



Source：OIF Next Generation CEI-224G Framework, OIF-FD-CEI-224G-01,February 7, 2022

调制格式、波特率、SNR的挑战

Table 3 Key parameters for different PAM schemes

Data rate, Gbps	112	224					
Number of PAM levels	**4**	**4**	**5**	**6**	**7**	**8**	**16**
Bits per symbol *	2	2	2.25	2.5	2.75	3	4
Signaling rate, GBd	56.25	112.5	100	90	81.82	75	56.25
Unit interval, ps	17.78	8.89	10	11.11	12.22	13.33	17.78
Fundamental frequency, GHz	28.125	56.25	50	45	40.91	37.5	28.125
Required SNR at slicer, dB **	20.42	20.42	22.43	24.04	25.40	26.56	32.55
SNR penalty, dB	0	0	2.01	3.62	4.97	6.14	12.12

* Assumes an efficient mapping of bits to PAM symbols.
** For BER = 1e−6.

Source：OIF Next Generation CEI-224G Framework, OIF-FD-CEI-224G-01,February 7, 2022

更复杂DSP 和 FEC技术的挑战

Analog
High speed ADC enables DSP architecture

DSP
FFE, DFE, and MLSD for Stronger equalization

Coding
Leverage DSP soft information for higher coding gain FEC

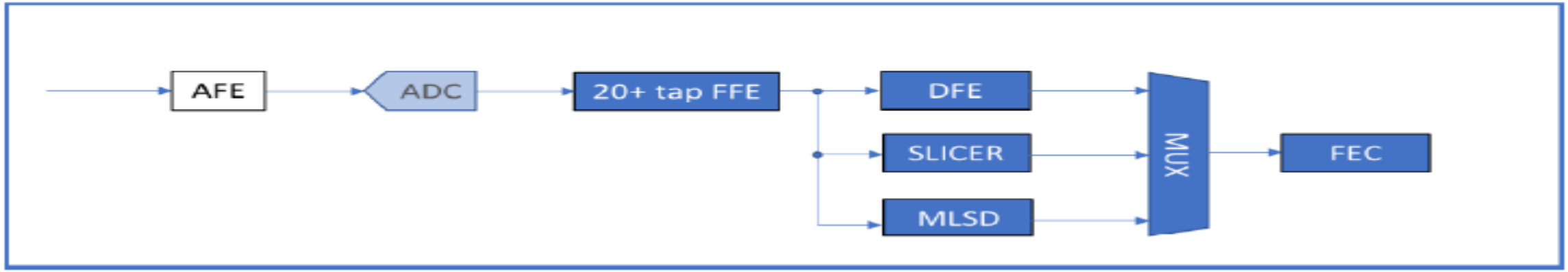


Figure 9 Block diagram of a DSP receiver

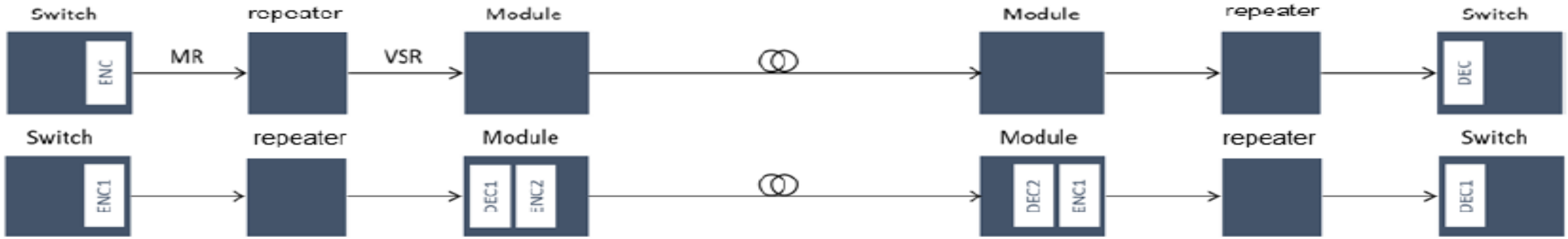


Figure 10 Shared FEC architecture (top) and Terminated FEC architecture (bottom)

KEYSIGHT

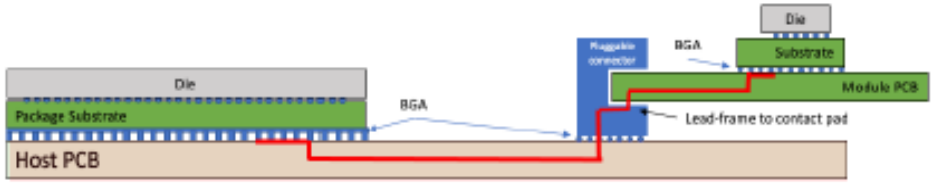
Source：OIF Next Generation CEI-224G Framework, OIF-FD-CEI-224G-01,February 7, 2022

通道的一致性测试的重要性

CEI – An Essential Building Block for Co-packaging

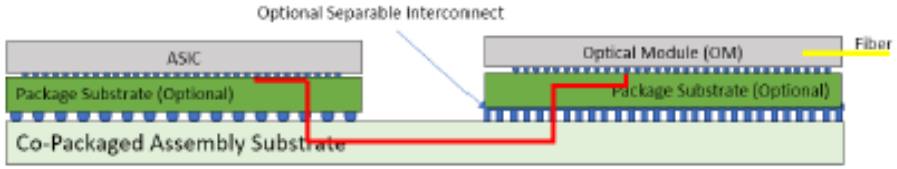
OIF CO-PACKAGING

Pluggable Module Channel Example Illustration



- Channel loss: 16dB ball to ball (22-24dB bump to bump)
- Typical pluggable connectors: IL of ~1dB with RL of -10dB @26.5GHz

CPO/NPO Channel Example Illustration



- Channel loss: CPO – 10dB bump to bump; NPO – 13dB bump to bump
- Optional separable interconnect performance example: LGA socket: IL of ~0.05dB with RL of -40dB @26.5GHz (*oif2020.341.01, Nathan Tracy*)
- Avoids/reduces major discontinuities.
- Optical modules are not end user pluggable.

- Significant power saving opportunity over VSR to be captured.
- A broad interoperable ecosystem is the key to success and can only be achieved through standardization.

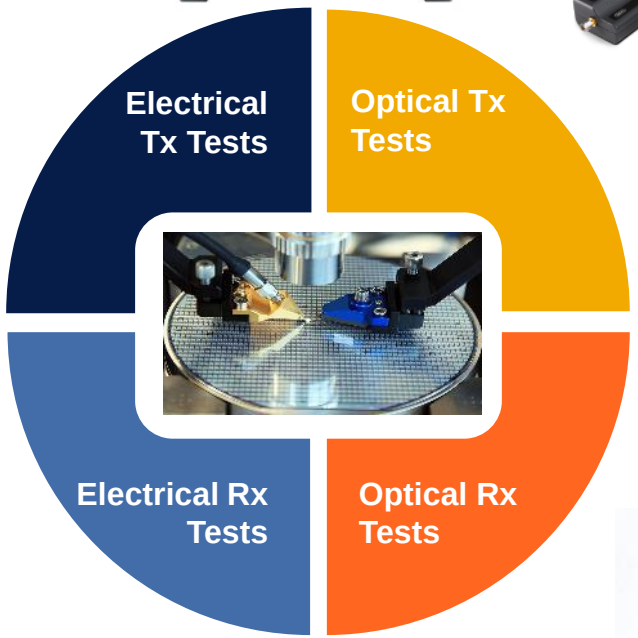
Source：*OIF Co-Packaging Interoperability Demo in OFC 2022*

针对224 Gbps / 1.6T 技术的测试解决方案

UXR RTS
Up 110GHZ BW

N7005A UXR probe
60 GHz BW brickwall

N1046A Remote Sampling Heads
>100 GHz BW



N1032A/B
Optical Reference Receiver
120+ GHz BW

NEW!

M8050A BERT
120 Gbaud **NEW!**

M8199B AWG
256 GS/s & 80 GHz **NEW!**

N4372E LCA & N5290A VNA
110 GHz

M8199A AWG
256 GS/s & 65 GHz BW

224G信号在采样示波器里的测量案例

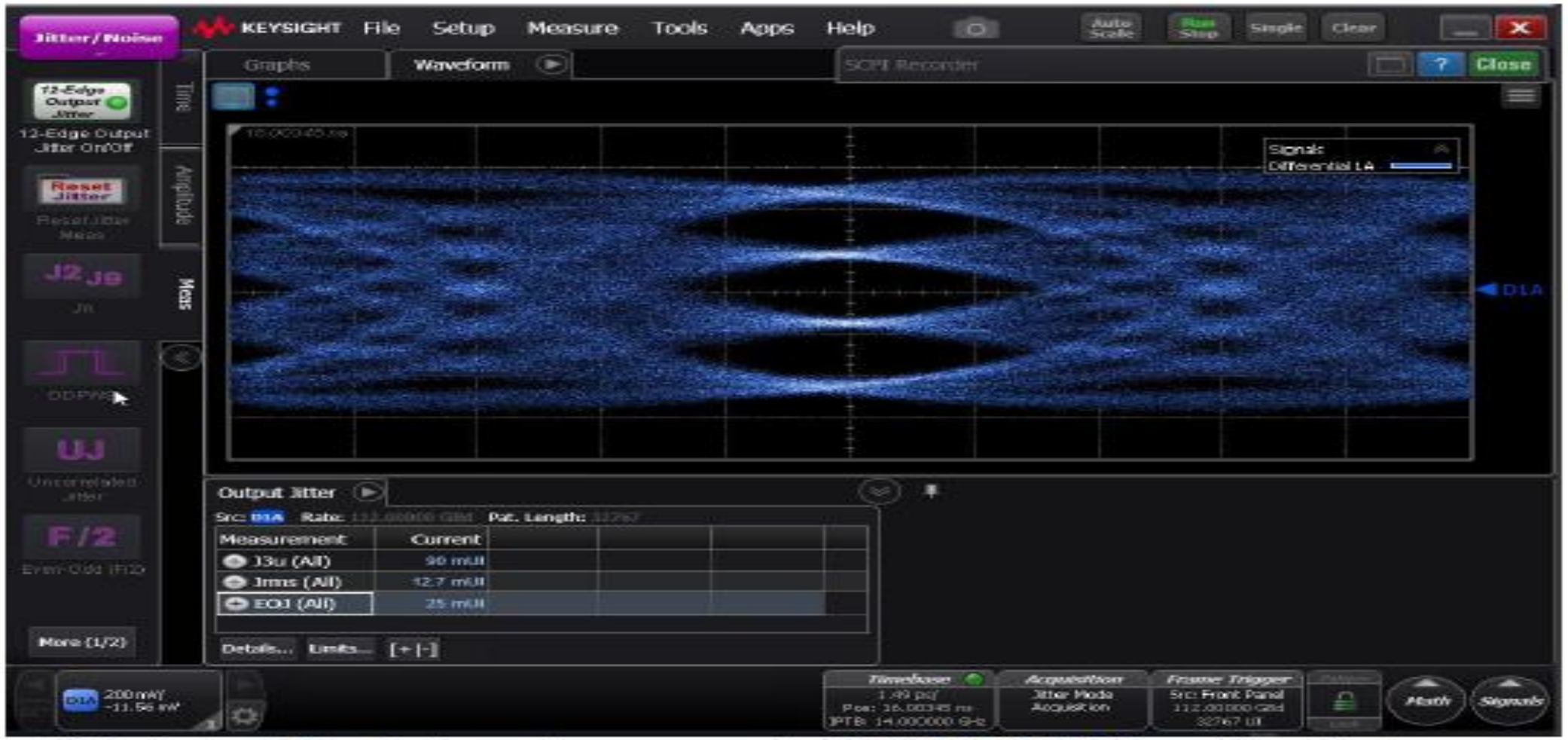


Figure 15 Equivalent-Time instrument measurement of a 112 GBd PAM4 precision stimulus

Source：OIF Next Generation CEI-224G Framework, OIF-ED-CEI-224G-01,February 7, 2022

224G信号在实时示波器里的测量案例

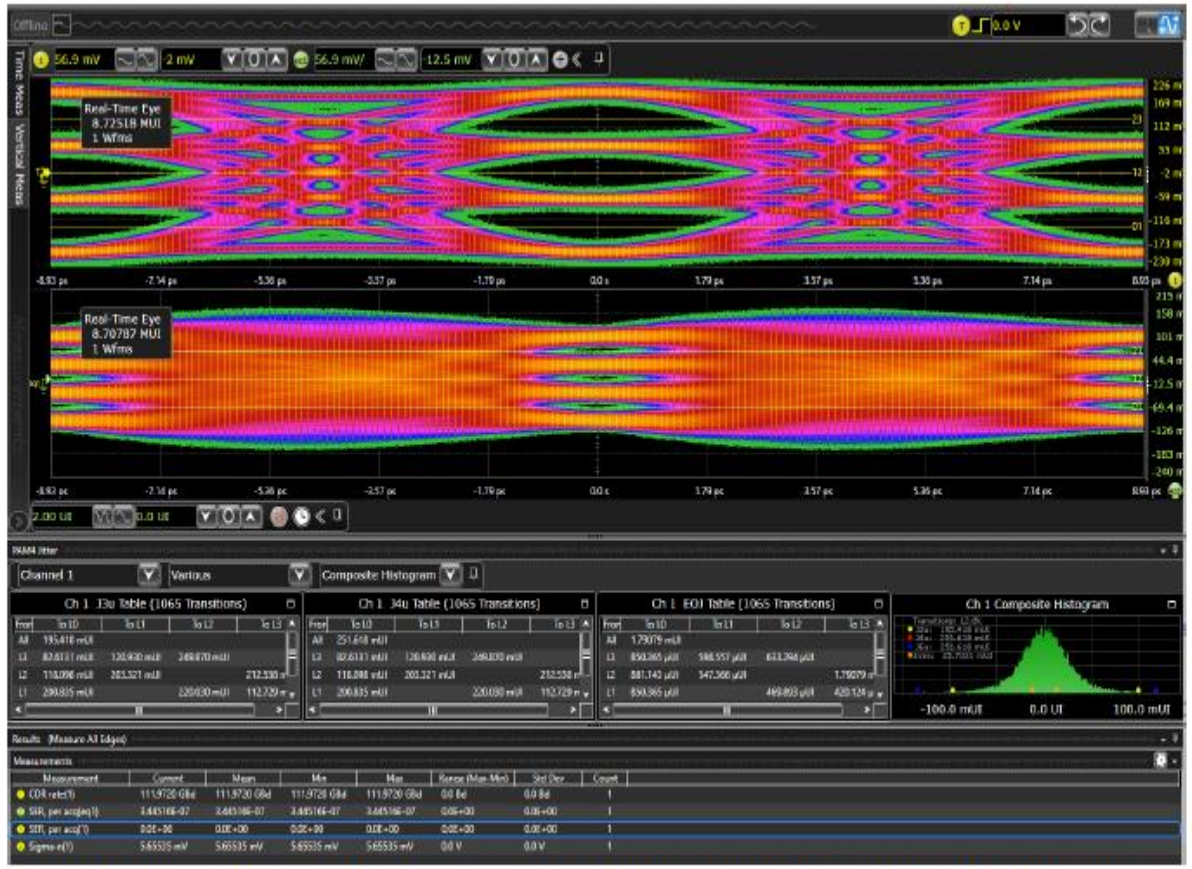


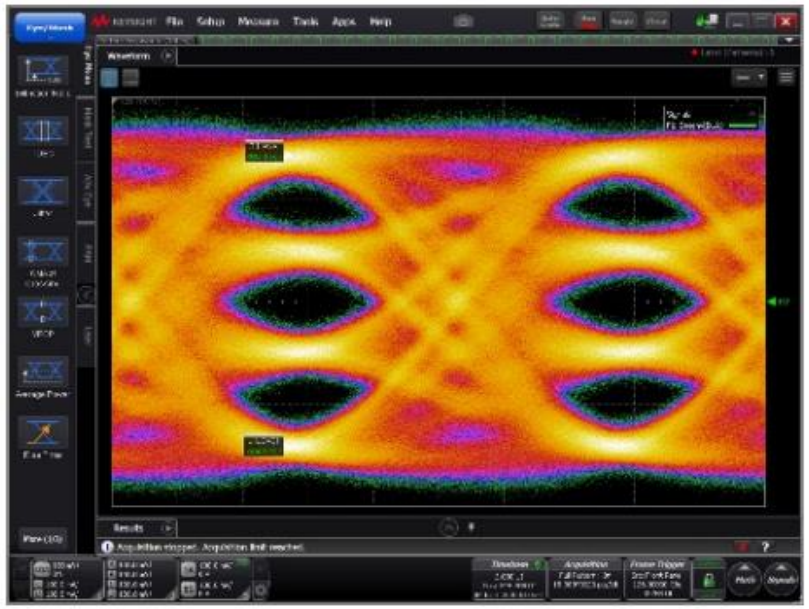
Figure 13 Real-Time instrument measurement of a 112 GBd PAM4 precision stimulus system incident to the illustrated packages

Measurement	Current
CDR rate(1)	111.9720 GBd
SER, per acq(eq1)	3.44516E-07
SER, per acq(1)	0.0E+00
Sigma-n(1)	5.65535 mV

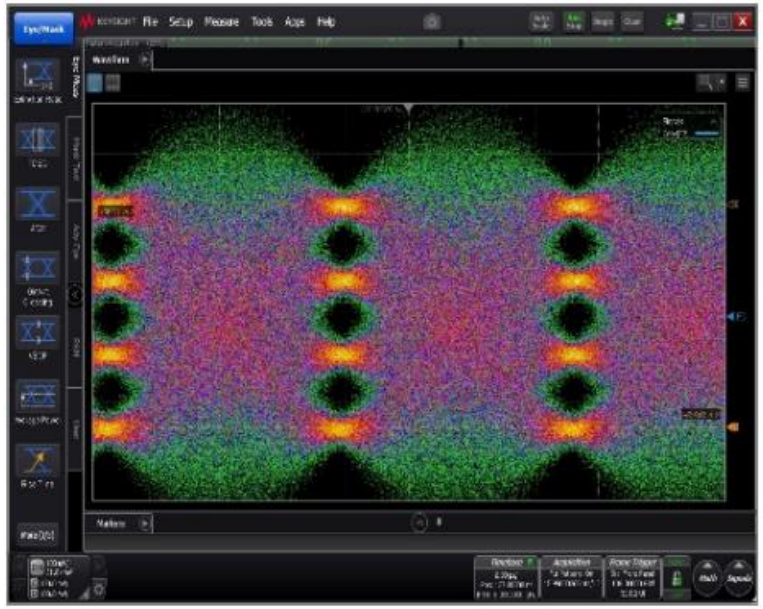
Figure 14 Equalization configuration for 112 GBd PAM4

Source：OIF Next Generation CEI-224G Framework, OIF-ED-CEI-224G-01,February 7, 2022

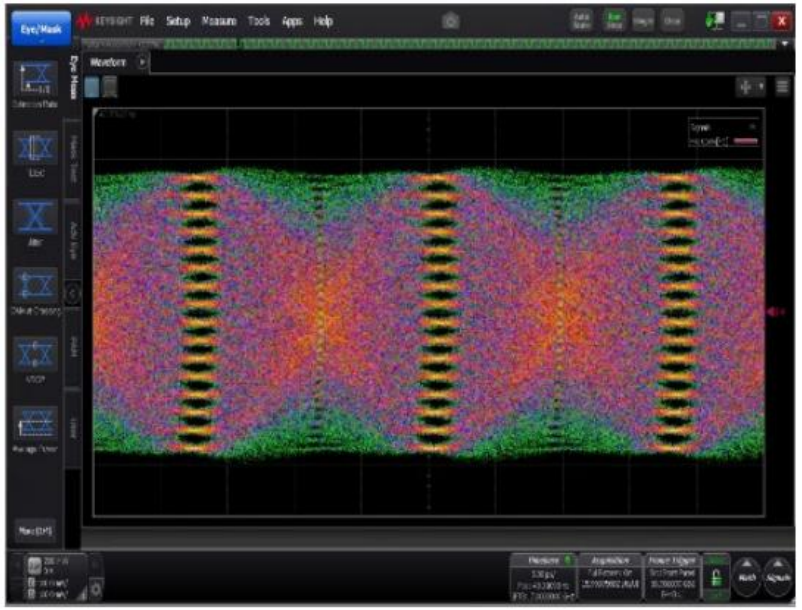
多制式 224Gbps+ 信号的产生和分析



PAM-4, 128 GBd (256 Gbps)



PAM-4, 136 GBd (272 Gbps)



PAM-16, 56 GBd (224 Gbps)

M8199A AWG

- 70 GHz BW
- 256 GSa/s
- 2/4 Channels

M8199B AWG

- 80 GHz BW
- 256 GSa/s
- 2/4 Channels

N1000A+ N1046A DCA

- >100GHz BW
- HW de-skew
- 1/2/4 Channels

M8199A vs M8199B

Specification/Criteria	M8199B	M8199A with ILV	M8199A without ILV
Sample rate	200 to 256 GSa/s	200 to 256 GSa/s	100 to 128 GSa/s
DAC resolution	8 bits	8 bits	8 bits
Number of channels per module	1 channel (option -001) or 2 channels (option -002)	1 channel (option -002) or 2 channels (option -004)	2 channels (option -002) or 4 channels (option -004)
Analog bandwidth – including sin(x)/x roll off	75 GHz @ 3dB 80 GHz @ 6dB 90 GHz @ 10dB	55 GHz @ 3dB 67 GHz @ 6dB >70 GHz @ 10dB* (with remote-head, *limited by 1.85mm connectors)	50 GHz @ 3dB 65 GHz @ 6dB >70 GHz @ 10dB* (*limited by 1.85mm connectors)
Amplitude Range	300 $mV_{pp, se}$ to 2.5 $V_{pp, se}$ into 50 Ω 600 $mV_{pp, diff}$ to 5.0 $V_{pp, diff}$ into 50 Ω (at 100 MHz)	100 $mV_{pp, se}$ to 0.625 $V_{pp, se}$ into 50 Ω 200 $mV_{pp, diff}$ to 1.25 $V_{pp, diff}$ into 50 Ω (at 400 MHz)	100 $mV_{pp, se}$ to 0.83 $V_{pp, se}$ into 50 Ω 200 $mV_{pp, diff}$ to 1.66 $V_{pp, diff}$ into 50 Ω (at 400 MHz)
Achievable amplitude	3.0 $V_{pp, diff}$ @ 128 GBd 2.0 $V_{pp, diff}$ @ 160 GBd	0.6 $V_{pp, diff}$ @ 128 GBd 0.4 $V_{pp, diff}$ @ 136 GBd	1.4 $V_{pp, diff}$ @ 128 GBd
Sample memory	1024 kSa per channel	1024 kSa pers channel	512 kSa per channel
Waveform granularity	512 samples	512 samples	256 samples
Connector type	1.00 mm	1.85 mm	1.85 mm
Clock Module	M8008A	M8008A	M8008A

M8050A 误码仪与UXR示波器联合120GBd误码测试系统

SD7150A = M8050A BERT + UXR-Series oscilloscope

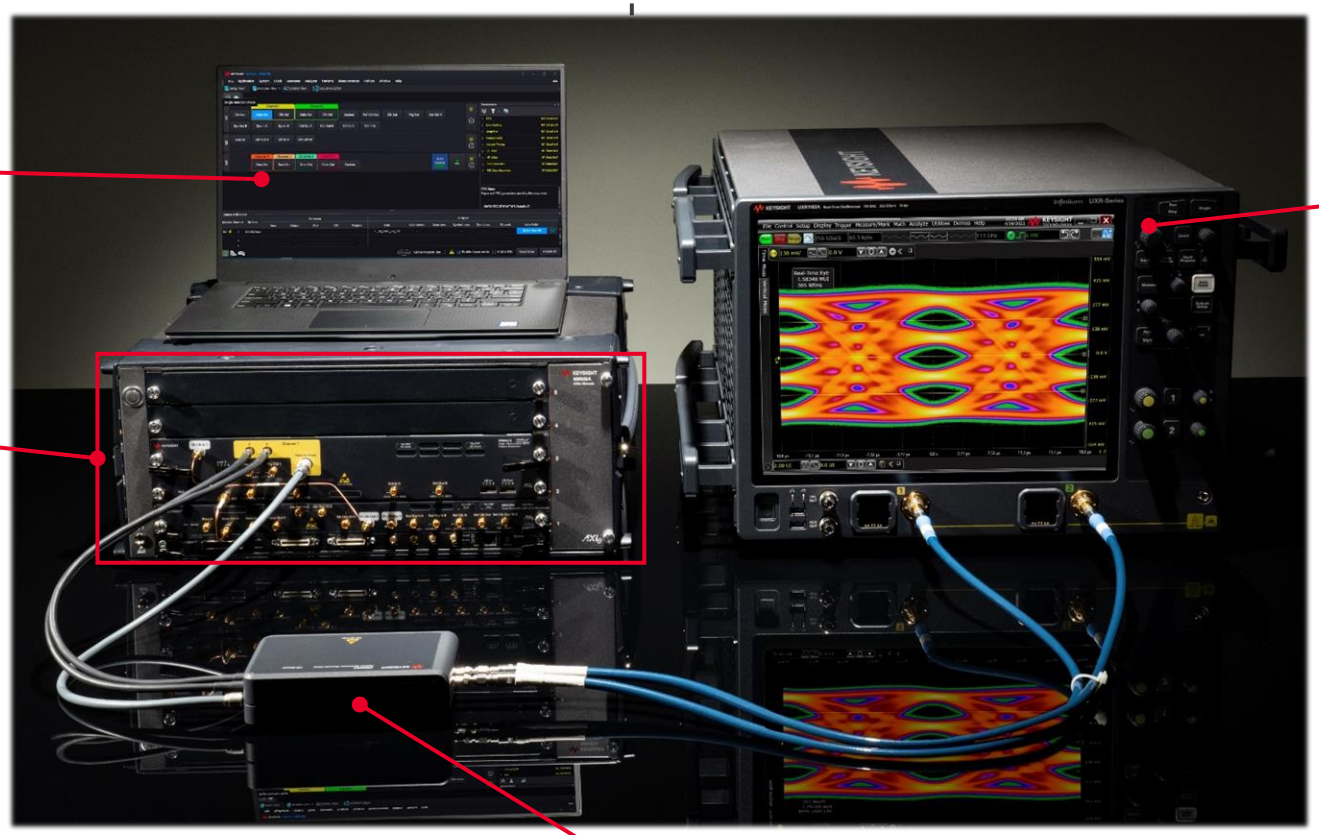
Pattern Generator (PG) ⟷ **Error Detector (ED)**

PC Software
M8070x control,
measurement, & analysis

M8050A BERT

M8042A 120 GBd PG Module
1 channel + 2 slots (shown)
2 channel + 3 slots

M8009A Clock Module
Includes jitter modulation
+ 1 slot



UXR-Series Oscilloscope
Minimum 80 GHz bandwidth
2- or 4-channels

Pattern Generator Remote Head:
M8058A – Up to 64 GBd
M8059A – Up to 120 GBd

224Gbps+ 光/电信号链路误码分析实例

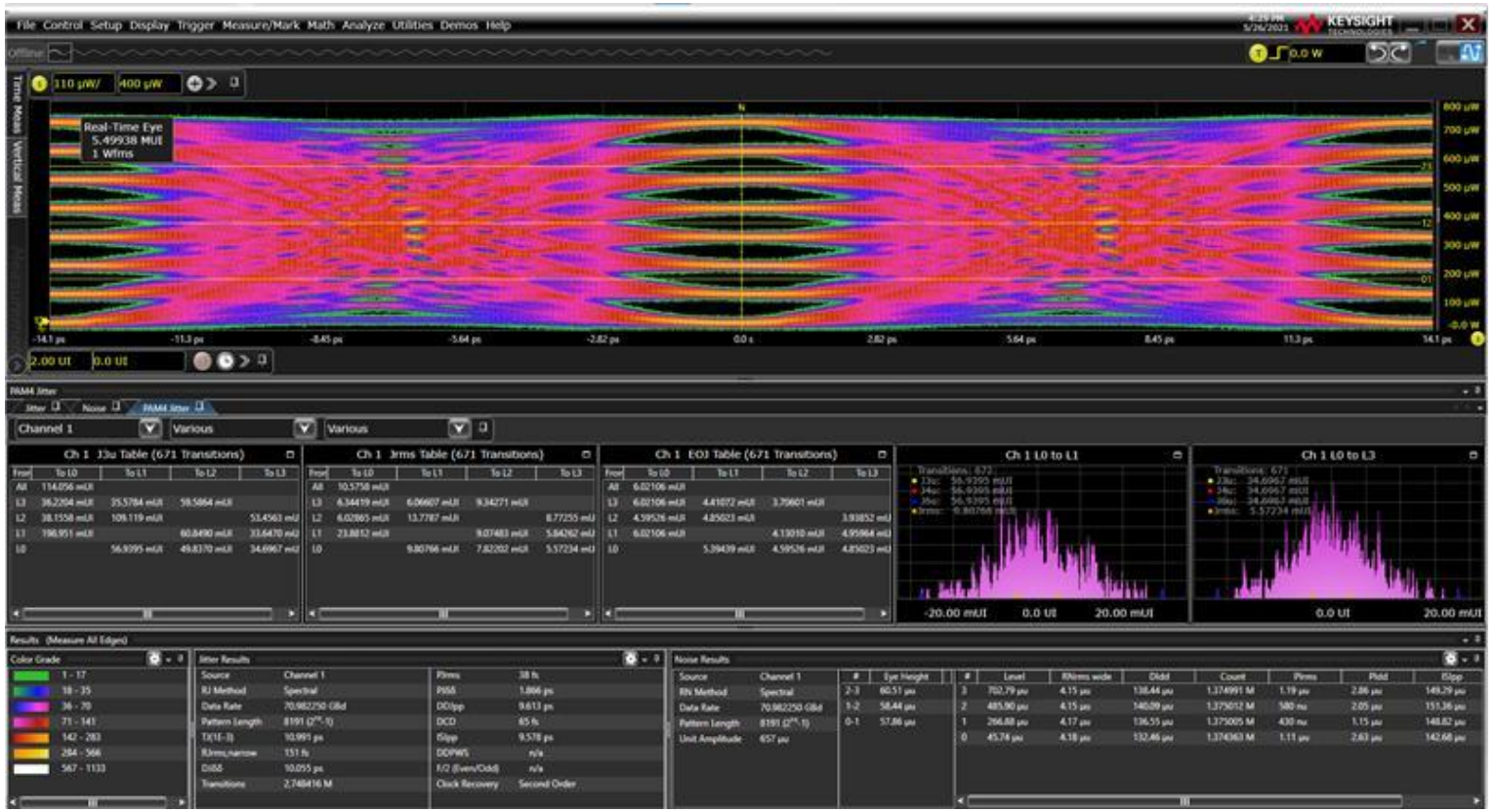
224 Gbps

- **FlexRT** in concert with the N7005A 60 GHz O/E converter, offers the convenient look and feel of the FlexDCA user experience along with the familiar optical measurements**.**

- **Infiniium UXR Series real-time oscilloscopes** provide convenient PAM4, PAM6 and PAM8 clock recovery, and advanced edge analysis (Jnu, Jrms, EOJ) based on programable edge definitions.

- Error Detection at these higher order modulation levels up to 224 Gbps

Measurement		Current	Minimum	Maximum	Count
Outer OMA	1A	824.6 µW	824.6 µW	836.2 µW	2
TDECQ	F1	1.76 dB	1.76 dB	1.77 dB	2
Ceq	F1	0.33 dB	0.33 dB	0.33 dB	2
Trans. Time (Slowest; 4,5)	1A	11.0 ps	11.0 ps	11.0 ps	2
Average Power	1A	789.91 µW	789.91 µW	790.42 µW	2



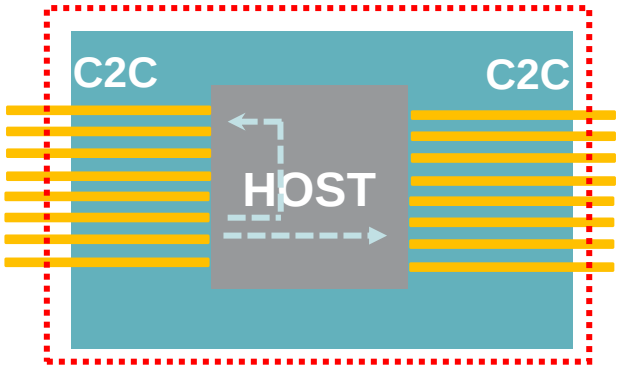
70.8GBd PAM8 with Nyquist at 35.4GHz

举例：单通道224G的交换机或Phy芯片测试

- **M8050A BERT** – BERT platform up to 120 GBd (NRZ, PAM4, PAM6, PAM8) **NEW!**
- UXR0802A or UXR0804A

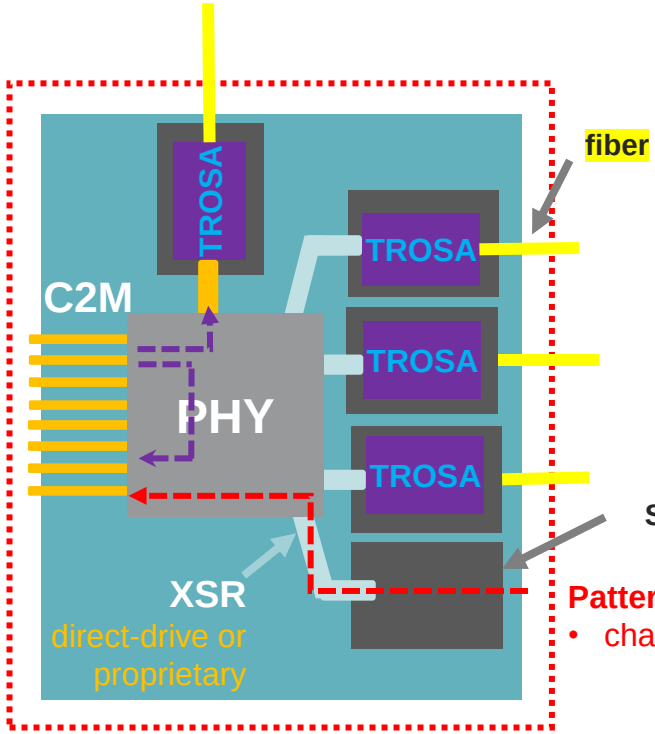
Error Detector
- 10dB equalization
- sensitivity <10mV Eye

Pattern Generator
- Interference noise
- sinusoidal jitter (SJ)
- Adjustable Linearity



Pattern Generator
- Adjustable ISI,
- Sin., random and bounded uncorrelated Jitter ,

Error Detector:
- 7dB equalization
- Sensitivity <5mV Eye



Pattern Generator
- channel de/embedding

举例：224G的C2M传输通道测试

N5290A

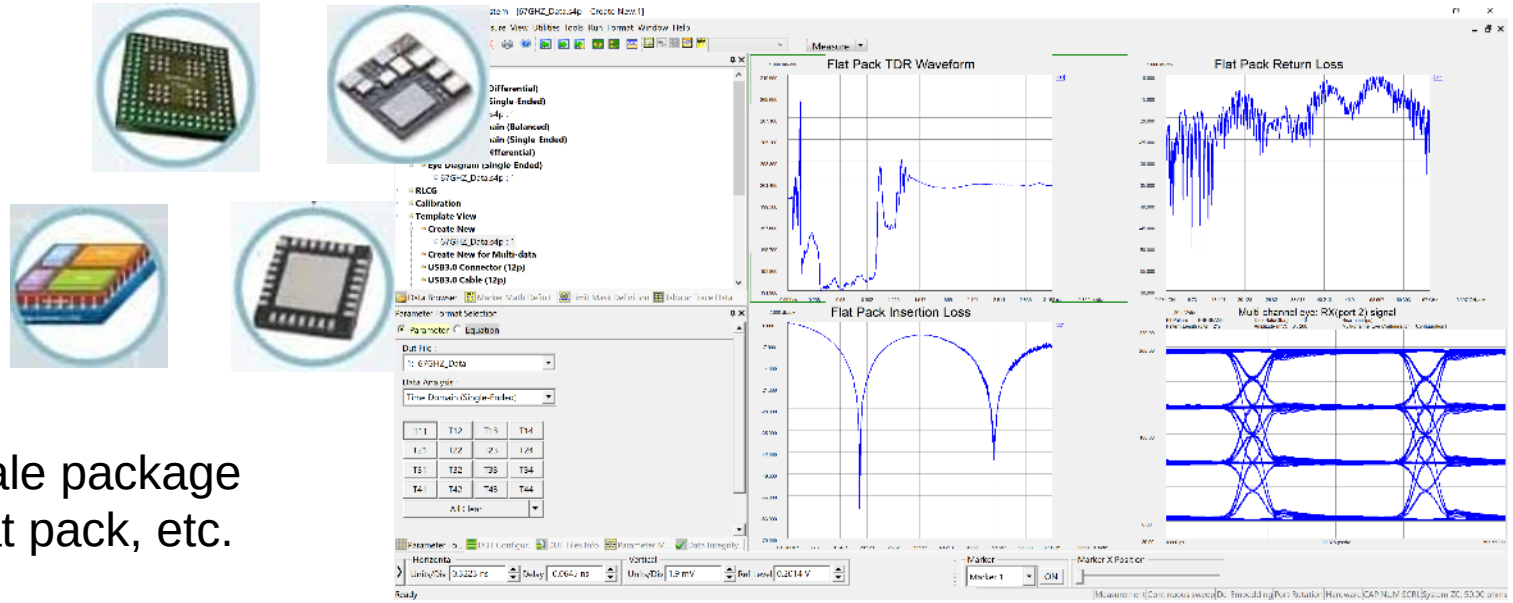
- 4-port 120 GHz VNA for highest accuracy
- Powerful de-embedding with Automatic Fixture Removal
- Industry best sub-millimeter spatial resolution

Applications

- OIF-CEI 224G
- OSFPmsa-200GeI
- 90Gbd PAM6 / 112Gbd PAM4

Challenges

- 100Ω → 85 Ω
- 70GHz+ analysis
- Probing
- IL deviation



DUT

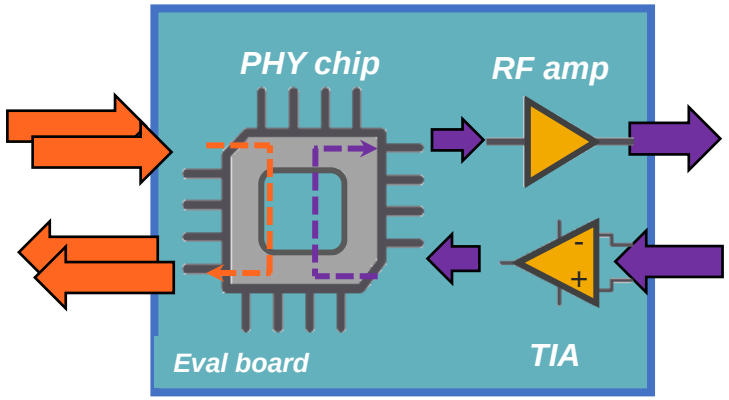
- ASICs
- Chip-scale package
- Quad flat pack, etc.

举例：224G GearBox芯片测试

M8050A BERT
- BER
- Jtol
- Burst

UXR RTS
- Waveform analysis
- Error counting
- SW CDR
- Rx emulation
- PAM4/PAM6

224G GearBox芯片



***112 Gbps** Tx & Rx conformance test e.g. IEEE 802.3ck*

***224 Gbps** waveform analysis & validation*

N1060A DCA or UXR RTS
- VEC
- Jnu, EOJ
- SNDR

M8199A AWG or M8050A BERT
- Channel & component embedding
- PAM4/PAM6

举例：下一代TOSA器件测试

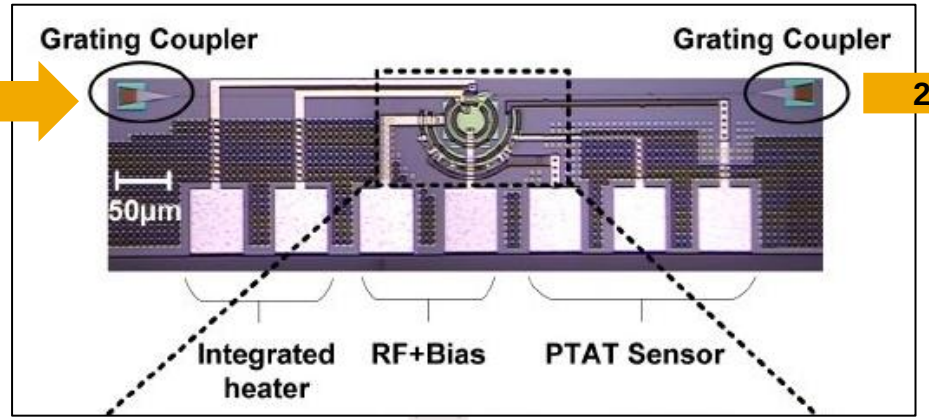
N77xxC Optical Component Test Instruments

- N7776C Tunable Laser Source
- N7745C Multiport Power Meters
- N7786C Polarization Synthesizer

E36300 Series

Triple Output Power Supply

基于硅光的微环调制器



Picture from [1]

CW

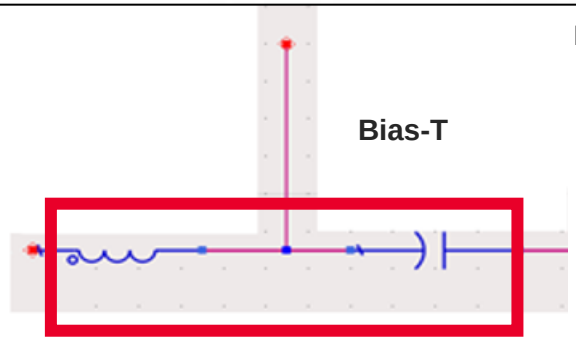
200G/λ

DCA-X Sampling Oscilloscopes

- N1000A DCA-X Mainframe
- N1032A/B Optical mini-module

M8199A AWG

- 128/256 Gsa/s
- Arbitrary Waveform Generator



DC

80 GBd PAM6

[1] Saman Saeedi and Azita Emami, "Silicon-photonic PTAT temperature sensor for micro-ring resonator thermal stabilization," Opt. Express **23**, 21875-21883 (2015)

KEYSIGHT

Thank you